generating a hardware description based on the block diagram of the graphical program, wherein the hardware description describes a hardware implementation of the block diagram;

configuring the programmable hardware element in the device utilizing the hardware description to produce a configured programmable hardware element, wherein the configured programmable hardware element implements a hardware implementation of the block diagram;

the device acquiring a signal from an external source after said configuring;

the measurement system executing to perform the measurement function, wherein the measurement system executing includes the configured programmable hardware element executing to control one or more operations of the measurement function; and

displaying one or more panels on a display during the measurement system executing to perform the measurement function on the signal, wherein at least one of the one or more panels displays the signal.

73. The method of claim 72,

wherein at least one of the one or more panels displays output from the device during said executing.

74. The method of claim 72,

wherein at least one of the one or more panels is operable to receive user input for providing input to the configured programmable hardware element during said executing.

75. The method of claim 74, further comprising:

receiving user input to the at least one of the one or more panels during said executing;

providing the user input to the configured programmable hardware element; and

the configured programmable hardware element adjusting control of the measurement function on the signal in response to the user input.

76. The method of claim 74,

wherein the one or more panels are useable for controlling the device and viewing output data from the device during the measurement system executing to perform the measurement function on the signal.

77. The method of claim 72,

wherein the device is coupled to a computer system, wherein the computer system includes the display;

wherein said displaying comprises the computer system executing software to display the one or more panels on the display during the configured programmable hardware element in the device executing to control one or more operations of the measurement function.

78. The method of claim 72, wherein the graphical program specifies the one or more panels;

the method further comprising:

compiling a portion of the graphical program corresponding to the one or more panels into executable code for execution by a computer system, wherein the computer system is coupled to the device.

79. The method of claim 72,

wherein said generating includes incorporating a register in the hardware description for at least one of the one or more panels;

wherein the configured programmable hardware element in the device executing to control one or more operations of the measurement function includes accessing a register on the configured programmable hardware element to affect values displayed in one of said one or more panels.

80. The method of claim 72, the method further comprising:

performing analog to digital conversion on the signal after said acquiring and prior to said executing.

81. The method of claim 72, wherein the device operates as an instrument.

82. The method of claim 72, wherein the device operates as a virtual instrument.

83. The method of claim 72, wherein the external source is a unit under test.

84. The method of claim 72, wherein the configured programmable hardware element in the device executes to perform a process control function using the signal.

85. The method of claim 72, wherein the configured programmable hardware element in the device executes to model a process.

86. The method of claim 72, wherein the device further includes timer/counter logic, the method further comprising:

the timer/counter logic performing one of timing / counting operations during the configured programmable hardware element in the device executing to control one or more operations of the measurement function.

87. The method of claim 72, further comprising:

converting the hardware description into a net list; and

compiling the net list format into a hardware program file;

wherein said configuring the programmable hardware element includes downloading the hardware program file to the programmable hardware element to configure the programmable hardware element.

88. The method of claim 87, wherein said converting the hardware description into a net list includes:

utilizing at least one function block from a library of pre-compiled function blocks; and

utilizing hardware target specific information.

89. The method of claim 72, wherein said creating the graphical program includes:

arranging on the screen a plurality of nodes comprising the graphical program;

creating and storing data structures which represent the graphical program in response to said arranging;

wherein said generating the hardware description comprises:

traversing the data structures;

converting the data structures into a hardware description format in response to said traversing.

90. The method of claim 72, wherein the graphical program includes a plurality of nodes;

wherein said generating the hardware description comprises converting each of said nodes into a hardware description format.

91. The method of claim 90, wherein each of said nodes is converted into a hardware description format including an enable input, a clock signal input, and an enable output;

wherein, for a respective node, said enable input receives an enable signal generated from enable out signals from one or more nodes which provide inputs to the respective node.

92. The method of claim 90, wherein the graphical program includes an input terminal;

wherein, for said input terminal, said converting comprises:

determining if data input to the input terminal is from one of said one or more panels;

creating a hardware description of a write register, wherein the write register includes one or more data outputs and at least control output.

93. The method of claim 90, wherein the graphical program includes a function node;

wherein, for said function node, said converting comprises:

determining inputs and outputs to/from the function node;

generating a hardware description of logic which performs the function indicated by the function node;

traversing input dependencies of the node;

creating a hardware description of an AND gate, including listing connections of said input dependencies of the node to said AND gate.

94. The method of claim 90, wherein the graphical program includes a structure node;

wherein, for said structure node, said converting comprises:

determining inputs and outputs to/from the structure node;

generating a hardware description of a control block which performs the control function indicated by the structure node;

traversing input dependencies of the node;

creating a hardware description of an AND gate, including listing connections of said input dependencies of the node to said AND gate.

95. The method of claim 90, wherein the graphical program includes an output terminal;

wherein, for said output terminal, said converting comprises:

determining if data output from the output terminal is to one of said one or more panels;

creating a hardware description of a read register, wherein the read register includes one or more data inputs and at least control input.

96. The method of claim 72, wherein the graphical program comprises a plurality of interconnected nodes which visually indicate functionality of the graphical program.

97. The method of claim 72, wherein the graphical program comprises a data flow diagram.

98. The method of claim 72, wherein a first portion of the block diagram portion is converted into a hardware description;

the method further comprising:

compiling a second portion of the block diagram portion into machine code for execution by the processor;

the configured programmable hardware element performing functionality indicated by the first portion of the block diagram portion;

executing the machine code to perform functionality indicated by the second portion of the block diagram portion;

wherein said executing the machine code and the configured programmable hardware element performing functionality operate to perform functionality indicated by the block diagram portion of the graphical program.

99. The method of claim 72, wherein the device includes a non-volatile memory coupled to the programmable hardware element, the method further comprising:

storing the hardware description into the non-volatile memory;

wherein said configuring the programmable hardware element comprises transferring the hardware description from the non-volatile memory to the programmable hardware element to produce the configured programmable hardware element.

100. A measurement system, comprising:

a computer system comprising a processor, memory and a display;

wherein the memory stores a graphical program, wherein the graphical program includes a block diagram, wherein the graphical program implements a function in the measurement system;

wherein the memory also stores a software program which is executable to generate a hardware description based on the block diagram of the graphical program, wherein the hardware description describes a hardware implementation of the block diagram of the graphical program; and

a device coupled to the computer system, wherein the device includes:

an input for acquiring a signal from an external source; and

a programmable hardware element, wherein the programmable hardware element in the device is configurable utilizing the hardware description to produce a configured programmable hardware element, wherein the configured programmable hardware element implements a hardware implementation of the block diagram of the graphical program, wherein the configured programmable hardware element in the device is executable to control one or more operations of a measurement function on an acquired signal;

wherein the computer system is operable to display one or more panels on the display while the configured programmable hardware element in the device executes to control one or more operations of the measurement function on the acquired signal, wherein at least one of the one or more panels displays the measured signal.

101. The measurement system of claim 100,

wherein at least one of the one or more panels displays output from the device during execution of the configured programmable hardware element in the device.

102. The measurement system of claim 100,

wherein at least one of the one or more panels is operable to receive user input for providing input to the configured programmable hardware element during said executing.

103. The measurement system of claim 102,

wherein the at least one of the one or more panels is operable to receive user input during execution of the configured programmable hardware element;

wherein the user input is operable to be provided to the configured programmable hardware element; and

wherein the configured programmable hardware element is operable to adjust control of the measurement function on the signal in response to the user input.

104. The measurement system of claim 102, wherein the graphical program specifies the one or more panels;

wherein the computer system is operable to compile a portion of the graphical program corresponding to the one or more panels into executable code for execution by the computer system.

105. The measurement system of claim 102,

wherein, in generating the hardware description based on the block diagram, the software program is operable to incorporate a register in the hardware description for at least one of the one or more panels;

wherein the programmable hardware element in the device is operable to access the register on the configured programmable hardware element to affect values displayed in one of said one or more panels.

106. The measurement system of claim 102, wherein the device further comprises:

analog to digital conversion logic coupled to the input and to the programmable hardware element for performing analog to digital conversion logic on an acquired analog signal to produce a digital signal.

107. The measurement system of claim 102, wherein the device further includes timer/counter logic;

wherein the timer/counter logic performs one of timing / counting operations while the configured programmable hardware element in the device executes to perform the measurement function on the signal.

108. The measurement system of claim 102, wherein the external source is a unit under test.

109. The measurement system of claim 102, wherein the configured programmable hardware element in the instrument executes to perform a process control function using the signal.

110. The measurement system of claim 102, wherein the software program stored in the memory of the computer system is further operable to convert the hardware description into a net list;

wherein the computer system is operable to configure the programmable hardware element utilizing the net list;

wherein the software program stored in the memory of the computer system is further operable to compile the net list format into a hardware program file; and

wherein the computer system is operable to download the hardware program file to the programmable hardware element to configure the programmable hardware element.

111. The measurement system of claim 102, wherein the programmable hardware element comprises a field programmable gate array (FPGA).

112. The measurement system of claim 102, wherein the computer system includes a bus and also includes one or more expansion slots coupled to the bus adapted for receiving expansion cards;

wherein the device comprises an expansion card inserted into an expansion slot of the bus.

113. The measurement system of claim 102, wherein the device is an external instrument coupled to the computer system.

114. The measurement system of claim 102, wherein the memory of the computer system stores a graphical programming system for creation of the graphical program;

wherein the graphical programming system is executable to arrange on the screen a plurality of nodes comprising the graphical program in response to user input;

wherein the graphical programming system is further executable to create and store data structures which represent the graphical program in response to said arranging;

wherein the software program is executable to traverse the data structures and convert the data structures into a hardware description format in response to said traversing.

115. The measurement system of claim 102, wherein a first portion of the block diagram portion is converted into a hardware description;

wherein the computer system is operable to compile a second portion of the block diagram portion into machine code for execution by the CPU.

116. The measurement system of claim 115,

wherein the configured programmable hardware element is operable to perform functionality indicated by the first portion of the block diagram portion;

wherein the computer system is operable to execute the machine code to perform functionality indicated by the second portion of the block diagram portion;

wherein said executing the machine code and the configured programmable hardware element performing functionality operate to perform functionality indicated by the block diagram portion of the graphical program.

117. The measurement system of claim 102, wherein the device includes a non-volatile memory coupled to the programmable hardware element;

wherein the non-volatile memory is operable to store the hardware description;

wherein the non-volatile memory is operable to transfer the hardware description to the programmable hardware element to produce the configured programmable hardware element.

118. The measurement system of claim 102, wherein the device performs data acquisition / generation functions.

119. The measurement system of claim 102, wherein the device is a GPIB instrument.

120. The measurement system of claim 102, wherein the device is a VXI instrument.

121. The measurement system of claim 102, wherein the device is a serial instrument.

122. The measurement system of claim 102, wherein the device is a programmable logic controller (PLC).

123. The measurement system of claim 102, wherein the device is a fieldbus device.

124. The measurement system of claim 102, wherein the block diagram comprises a plurality of interconnected nodes, wherein the plurality of interconnected nodes visually indicate functionality of the graphical program.

125. The measurement system of claim 124, wherein the plurality of interconnected nodes are connected to specify data flow among the nodes.

126. A. computer-implemented method for generating a hardware implementation of graphical code, the method comprising:

creating a graphical program, wherein the graphical program includes a plurality of interconnected nodes, wherein the interconnected nodes visually indicate functionality of the graphical program, wherein the graphical program implements control of a measurement function;

generating a hardware description based on the graphical program, wherein the hardware description describes a hardware implementation of the graphical program;

configuring a programmable hardware element utilizing the hardware description to produce a configured programmable hardware element, wherein the configured programmable hardware element implements a hardware implementation of the graphical program;

acquiring a signal from an external source after said configuring; and

the configured programmable hardware element executing to control the measurement function on the signal.

127. The method of claim 126, further comprising:

displaying one or more panels on a display during the configured programmable hardware element in the device executing to control the measurement function on the signal, wherein at least one of the one or more panels displays the measured signal.

128. The method of claim 127,

wherein the one or more panels are useable for viewing the signal.

129. The method of claim 127,

wherein the one or more panels are useable for providing input to and displaying output from the configured programmable hardware element.

130. The method of claim 127, further comprising:

storing executable code corresponding to the one or more panels in a memory, wherein the executable code is executable to display the one or more panels on a display;

a processor executing the executable code from the memory to present the one or more panels on the display during the configured programmable hardware element in the device executing to control the measurement function on the signal.

131. The method of claim 127, further comprising:

wherein the graphical program includes a block diagram and one or more panels, wherein the one or more panels operate as a user interface for the graphical program;

the method further comprising:

storing executable code corresponding to the one or more panels in a memory, wherein the executable code is executable to display the one or more panels on a display;

executing the executable code from the memory to present the one or more panels on the display during the configured programmable hardware element in the device executing to control the measurement function on the signal.

132. The method of claim 127,

wherein the graphical program comprises a data flow diagram;

wherein at least one of the nodes is a structure node which operates to control data flow in the graphical program.

133. The method of claim 127,

wherein the graphical program specifies one or more panels that operate as a user interface for the graphical program;

the method further comprising:

compiling a portion of the graphical program corresponding to the one or more panels into executable code for execution by a computer system;

wherein the programmable hardware element is comprised in a device;

wherein the computer system is coupled to the device.